DS26401DK
Octal T1/E1/J1 Framer Design Kit Daughter Card

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26401DK is an easy-to-use evaluation board for the DS26401 octal T1/E1/J1 framer. It is intended to be used as a daughter card with the DK101 motherboard or the DK2000 motherboard. The DS26401DK comes complete with a DS26401 octal framer, two DS21448 quad LIUs, transformers, termination resistors, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and the Dallas' ChipView software give point-and-click access to configurations and status registers from a Windows®-based PC. On-board LEDs indicate loss-of-signal, loss-of-frame, and interrupt status.

Each DS26401DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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DESIGN KIT CONTENTS

DS26401DK Board
DK101 Low-Cost Motherboard
CD-ROM
- ChipView Software
- DS26401DK Data Sheet
- DK101 Data Sheet
- DS26401 Data Sheet
- DS21448 Data Sheet
- DS26401 Errata Sheet

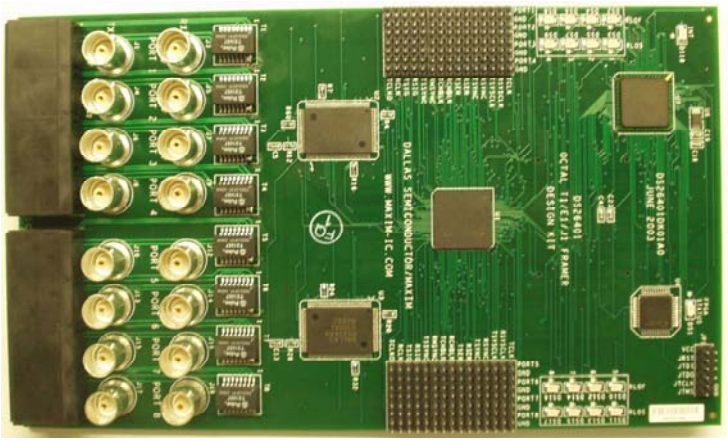
DS21448 Errata Sheet

FEATURES

- Demonstrates Key Functions of the DS26401 Octal T1/E1/J1 Framer
- Includes Two DS21448 Quad LIUs, Transformers, BNC and RJ45 Connectors, and Termination Passives
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS26401 Register Set
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- Memory-Mapped FPGA Provides Flexible Clock/Data/Sync Connections Among Framer Ports and DK2000 Motherboard
- LEDs for Loss-of-Signal, Loss-of-Frame, and Interrupt
- Easy-to-Read Silk-Screen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

ORDERING INFORMATION

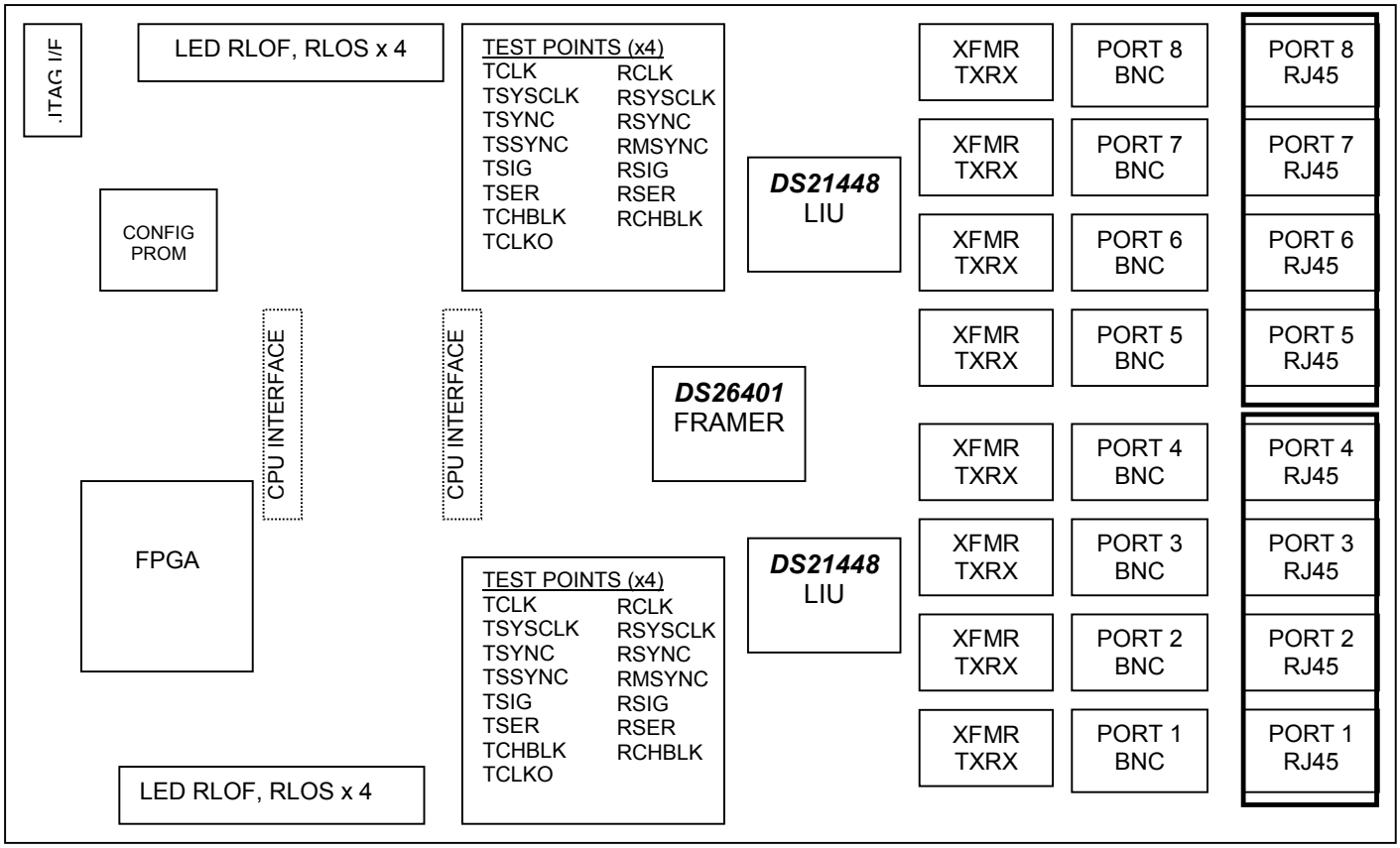
PART	DESCRIPTION
DS26401DK	DS26401 Demo Kit Daughter Card (with included DK101 motherboard)



COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C3, C5, C7, C9, C11, C13, C15, C17–C24, C26, C28–C31, C35–C42	29	00.1μF 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C2, C4, C6, C8, C10, C12, C14, C16	8	1μF 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
DS1, DS18	2	LED, green, SMD	Panasonic	LN1351C
DS2–DS17	16	LED, red, SMD	Panasonic	LN1251C
J1, J3–J10, J12-J18	16	5-pin connectors, 75Ω BNC vertical	Bourns	CP-BNCPC-004
J2, J11	2	Right-angle, RJ45 8-pin 4-port jack	3M Electronics	43223-8140
J19, J20	2	50-pin headers, socket, SMD dual row, vertical	Samtec	TFM-125-02-S-D-LC
J21, J23, J25, J27, J29, J31, J33, J35	8	20-pin headers, dual row, vertical	Samtec	HDR-TSW-110-14-T-D
J22, J24, J26, J28, J30, J32, J34, J36	8	10-pin headers, dual row, vertical	Murrietta	N/A
JP1	1	12-pin connector, dual row, vertical	Murrietta	N/A
R1, R2, R5, R6, R9, R10, R13, R14, R17, R18, R21, R22, R25, R26, R29, R30, R67	17	0Ω 1%, 1/16W resistors (0603)	AVX	CJ10-000F
R3, R4, R7, R8, R11, R12, R15, R16, R19, R20, R23, R24, R27, R28, R31, R32	16	60.4Ω 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF60R4V
R33–R35	3	10kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R36, R37, R68	3	330Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
R38, R59–R66	9	30.1Ω 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF30R1V
R39–R54	16	300Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ301V
R55–R58	4	10.0kΩ 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF1002V
T1–T8	8	XFMR, dual, 16-pin SMT	Pulse Engineering	TX1467
U1	1	Octal T1/E1/J1 framer	Dallas Semiconductor	DS26401
U2, U3	2	3.3V E1/T1/J1 quad LIU 128-pin LQFP, 0°C to +70°C	Dallas Semiconductor	DS21448L
U4	1	1M PROM for FPGA 44-pin TQFP	Xilinx	XC18V01VQ44C_U
U6	1	8-pin μMAX/SO 2.5V or Adj	Maxim	MAX1792EUA25
U7	1	XILINX Spartan 2.5V FPGA, 256-pin BGA	Xilinx	XC2S50-5FG256C

BOARD FLOORPLAN



QUICK SETUP (REGISTER VIEW)

- Connect DS26401DK to DK101 motherboard.
- Connect serial cable to a PC and DK101.
- Power DK101 with 3.3V.
- Load ChipView software.
- Select COM port.
- Select Register View.
- For T1 applications, load the *401_global_t1_DS26401DC.def* file. For E1 applications, load the *401_global_e1_DS26401DC.def* file.
- Make sure that all the register settings are correct for the proper function desired for the DS26401DK.

Please refer to the DS26401 data sheet (www.maxim-ic.com/DS26401) and the DS21448 data sheet (www.maxim-ic.com/DS21448) for all questions pertaining to device functionality.

ADDRESS MAP

DK101 daughter card address space begins at 0x81000000.
DK2000 daughter card address space begins at:

0x30000000 for slot 0
0x40000000 for slot 1
0x50000000 for slot 2
0x60000000 for slot 3

All offsets given below are relative to the beginning of the daughter card address space.

Table 1. Daughter Card Address Map

SPAN NUMBER	OFFSET		
	DS26401	DS21448	FPGA
1	0x1000	0x2000	0x10
2	0x1200	0x3000	0x20
3	0x1400	0x4000	0x30
4	0x1600	0x5000	0x40
5	0x1800	0x6000	0x50
6	0x1A00	0x7000	0x60
7	0x1C00	0x8000	0x70
8	0x1E00	0x9000	0x80

Registers in the FPGA can be easily modified using ChipView.exe host-based user-interface software along with the definition file named *DS26401DC_FPGA.def*.

FPGA REGISTER MAP

Table 2. FPGA Register map

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0010 0x0020 0x0030 0x0040 0x0050 0x0060 0x0070 0x0080	TSIG_SR –1 TSIG_SR –2 TSIG_SR –3 TSIG_SR –4 TSIG_SR –5 TSIG_SR –6 TSIG_SR –7 TSIG_SR –8	Control	DS26401 TSIG Pin Setting Port 1 DS26401 TSIG Pin Setting Port 2 DS26401 TSIG Pin Setting Port 3 DS26401 TSIG Pin Setting Port 4 DS26401 TSIG Pin Setting Port 5 DS26401 TSIG Pin Setting Port 6 DS26401 TSIG Pin Setting Port 7 DS26401 TSIG Pin Setting Port 8
0X0011 0X0021 0X0031 0X0041 0x0051 0x0061 0x0071 0x0081	TSER_SR –1 TSER_SR –2 TSER_SR –3 TSER_SR –4 TSER_SR –5 TSER_SR –6 TSER_SR –7 TSER_SR –8	Control	DS26401 TSER Pin Setting Port 1 DS26401 TSER Pin Setting Port 2 DS26401 TSER Pin Setting Port 3 DS26401 TSER Pin Setting Port 4 DS26401 TSER Pin Setting Port 5 DS26401 TSER Pin Setting Port 6 DS26401 TSER Pin Setting Port 7 DS26401 TSER Pin Setting Port 8
0X0012 0X0022 0X0032 0X0042 0X0052 0X0062 0X0072 0X0082	TSSYNC_SR –1 TSSYNC_SR –2 TSSYNC_SR –3 TSSYNC_SR –4 TSSYNC_SR –5 TSSYNC_SR –6 TSSYNC_SR –7 TSSYNC_SR –8	Control	DS26401 TSSYNC Source Port 1 DS26401 TSSYNC Source Port 2 DS26401 TSSYNC Source Port 3 DS26401 TSSYNC Source Port 4 DS26401 TSSYNC Source Port 5 DS26401 TSSYNC Source Port 6 DS26401 TSSYNC Source Port 7 DS26401 TSSYNC Source Port 8
0X0013 0X0023 0X0033 0X0043 0X0053 0X0063 0X0073 0X0083	TSYSCLK –1 TSYSCLK –2 TSYSCLK –3 TSYSCLK –4 TSYSCLK –5 TSYSCLK –6 TSYSCLK –7 TSYSCLK –8	Control	DS26401 TSYSCLK Source Port 1 DS26401 TSYSCLK Source Port 2 DS26401 TSYSCLK Source Port 3 DS26401 TSYSCLK Source Port 4 DS26401 TSYSCLK Source Port 5 DS26401 TSYSCLK Source Port 6 DS26401 TSYSCLK Source Port 7 DS26401 TSYSCLK Source Port 8
0X0014 0X0024 0X0034 0X0044 0X0054 0X0064 0X0074 0X0084	RSYSCLK –1 RSYSCLK –2 RSYSCLK –3 RSYSCLK –4 RSYSCLK –5 RSYSCLK –6 RSYSCLK –7 RSYSCLK –8	Control	DS26401 RSYSCLK Source Port 1 DS26401 RSYSCLK Source Port 2 DS26401 RSYSCLK Source Port 3 DS26401 RSYSCLK Source Port 4 DS26401 RSYSCLK Source Port 5 DS26401 RSYSCLK Source Port 6 DS26401 RSYSCLK Source Port 7 DS26401 RSYSCLK Source Port 8

Table 2. Register Map (continued)

OFFSET	NAME	TYPE	DESCRIPTION
0X0015	TCLK –1	Control	DS26401TCLK Source Port 1
0X0025	TCLK –2		DS26401TCLK Source Port 2
0X0035	TCLK –3		DS26401TCLK Source Port 3
0X0045	TCLK –4		DS26401TCLK Source Port 4
0X0055	TCLK –5		DS26401TCLK Source Port 5
0X0065	TCLK –6		DS26401TCLK Source Port 6
0X0075	TCLK –7		DS26401TCLK Source Port 7
0X0085	TCLK –8		DS26401TCLK Source Port 8
0X0016	RSYNC –1	Control	DS26401RSYNC Source Port 1
0X0026	RSYNC –2		DS26401RSYNC Source Port 2
0X0036	RSYNC –3		DS26401RSYNC Source Port 3
0X0046	RSYNC –4		DS26401RSYNC Source Port 4
0X0056	RSYNC –5		DS26401RSYNC Source Port 5
0X0066	RSYNC –6		DS26401RSYNC Source Port 6
0X0076	RSYNC –7		DS26401RSYNC Source Port 7
0X0086	RSYNC –8		DS26401RSYNC Source Port 8
0X0017	TSYNC –1	Control	DS26401TSYNC Source Port 1
0X0027	TSYNC –2		DS26401TSYNC Source Port 2
0X0037	TSYNC –3		DS26401TSYNC Source Port 3
0X0047	TSYNC –4		DS26401TSYNC Source Port 4
0X0057	TSYNC –5		DS26401TSYNC Source Port 5
0X0067	TSYNC –6		DS26401TSYNC Source Port 6
0X0077	TSYNC –7		DS26401TSYNC Source Port 7
0X0087	TSYNC –8		DS26401TSYNC Source Port 8
0X0090	CLK	Control	LIU MCLK and REF CLK Source

ID Registers

BID: BOARD ID (Offset = 0X0000)

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x1.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0x6.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: PLD REVISION (Offset = 0X0007)

PREV is read-only and displays the current PLD firmware revision.

Control Registers

Register Name: **TSIG_SR**
Register Description: **DS26401 TSIG x Pin Setting**
Register Offset: **0x0010, 0x0020, 0x0030, 0x0040, 0x0050, 0x0060, 0x0070, 0x0080**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Bit 0 to 7: DS26401 Port x TSIG Source (D7, D6, D5, D4, D3, D2, D1, D0)

The source for TSER is Defined as shown in Table 3.

Table 3. TSERx Source Definition

D3, D2, D1, D0	TSIG CONNECTION
0000	Tri-state TSIG
0001	Drive TSIG with RSIG1
0010	Drive TSIG with RSIG2
0011	Drive TSIG with RSIG3
0100	Drive TSIG with RSIG4
0101	Drive TSIG with RSIG5
0110	Drive TSIG with RSIG6
0111	Drive TSIG with RSIG7
1000	Drive TSIG with RSIG8
1010	Drive TSIG with T1 OSC
1011	Drive TSIG with E1 OSC
1100	Drive TSIG with 16.384MHz
1101	Drive TSIG with a logic 0
1110	Drive TSIG with a logic 1
1111	Tri-state TSIG

Note: Initial values are such that all values are tri-stated.

Register Name: **TSER_SR**
Register Description: **DS26401 TSERx Pin Setting**
Register Offset: **0x0011, 0x0021, 0x0031, 0x0041, 0x0051, 0x0061, 0x0071, 0x0081**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 3: DS26401 Port x TSER Source (D3, D2, D1, D0)

The source for TSER is Defined as shown in Table 4.

Table 4. TSERx Source Definition

D3, D2, D1, D0	TSER CONNECTION
0000	Tri-state TSER
0001	Drive TSER with RSER1
0010	Drive TSER with RSER2
0011	Drive TSER with RSER3
0100	Drive TSER with RSER4
0101	Drive TSER with RSER5
0110	Drive TSER with RSER6
0111	Drive TSER with RSER7
1000	Drive TSER with RSER8
1010	Drive TSER with T1 OSC
1011	Drive TSER with E1 OSC
1100	Drive TSER with 16.384MHz
1101	Drive TSER with a logic 0
1110	Drive TSER with a logic 1
1111	Tri-state TSER

Note: Initial values are such that all ports are tri-stated.

Register Name: **TSSYNC_SR**
Register Description: **DS26401 TSSYNCx Pin Setting**
Register Offset: **0x0012, 0x0022, 0x0032, 0x0042, 0x0052, 0x0062, 0x0072, 0x0082**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0
Default	0	0	0	0	0	1	0	1

Bit 0 to 2: DS26401 Port x TSSYNC Source (D3, D2, D1, D0)

The source for TSSYNC is Defined as shown in Table 5.

Table 5. TSSYNCx Source Definition

D3, D2, D1, D0	TSSYNC CONNECTION
0000	Tri-state TSSYNC
0001	Drive TSSYNC with RMSYNC1
0010	Drive TSSYNC with RMSYNC2
0011	Drive TSSYNC with RMSYNC3
0100	Drive TSSYNC with RMSYNC4
0101	Drive TSSYNC with RMSYNC5
0110	Drive TSSYNC with RMSYNC6
0111	Drive TSSYNC with RMSYNC7
1000	Drive TSSYNC with RMSYNC8
1010	Drive TSSYNC with T1 OSC
1011	Drive TSSYNC with E1 OSC
1100	Drive TSSYNC with 16.385MHz
1101	Drive TSSYNC with a logic 0
1110	Drive TSSYNC with a logic 1
1111	Tri-state TSSYNC

Note: Initial values are such that all ports are tri-stated.

Register Name: **TSYSCLK_SR**
Register Description: **DS26401 TSYSCLKx Pin Setting**
Register Offset: **0x0013, 0x0023, 0x0033, 0x0043, 0x0053, 0x0063, 0x0073, 0x0083**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x TSYSCLKC Source (D3, D2, D1, D0)

The source for TSYSCLK is Defined as shown in Table 6.

Table 6. TSYCLKx Source Definition

D3, D2, D1, D0	TSYSCLK CONNECTION
0000	Tri-state TSYSCLK
0001	Drive TSYSCLK with RCHBLK 1
0010	Drive TSYSCLK with RCHBLK 2
0011	Drive TSYSCLK with RCHBLK 3
0100	Drive TSYSCLK with RCHBLK 4
0101	Drive TSYSCLK with RCHBLK 5
0110	Drive TSYSCLK with RCHBLK 6
0111	Drive TSYSCLK with RCHBLK 7
1000	Drive TSYSCLK with RCHBLK 8
1001	BPCLK
1010	Drive TSYSCLK with T1 OSC
1011	Drive TSYSCLK with E1 OSC
1100	Drive TSYSCLK with 16.385MHz
1101	Drive TSYSCLK with a logic 0
1110	Drive TSYSCLK with a logic 1
1111	Tri-state TSYSCLK

Note: Initial values are such that all ports are tri-stated.

Register Name: **RSYSCLK_SR**
Register Description: **DS26401 RSYSCLKx Pin Setting**
Register Offset: **0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x RSYSCLKC Source (D3, D2, D1, D0)

The source for RSYSCLK is Defined as shown in Table 7.

Table 7. RSYSCLKx Source Definition

D3, D2, D1, D0	RSYSCLK CONNECTION
0000	Tri-state RSYSCLK
0001	Drive RSYSCLK with TCHBLK 1
0010	Drive RSYSCLK with TCHBLK 2
0011	Drive RSYSCLK with TCHBLK 3
0100	Drive RSYSCLK with TCHBLK 4
0101	Drive RSYSCLK with TCHBLK 5
0110	Drive RSYSCLK with TCHBLK 6
0111	Drive RSYSCLK with TCHBLK 7
1000	Drive RSYSCLK with TCHBLK 8
1001	BPCLK
1010	Drive RSYSCLK with T1 OSC
1011	Drive RSYSCLK with E1 OSC
1100	Drive RSYSCLK with 16.385MHz
1101	Drive RSYSCLK with a logic 0
1110	Drive RSYSCLK with a logic 1
1111	Tri-state RSYSCLK

Note: Initial values are such that all ports are tri-stated.

Register Name: **TCLK_SR**
Register Description: **DS26401 TCLKx Pin Setting**
Register Offset: **0x0015, 0x0025, 0x0035, 0x0045, 0x0055, 0x0065, 0x0075, 0x0085**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x TCLK Source (D3, D2, D1, D0)

The source for TCLK is Defined as shown in Table 8.

Table 8. TCLKx Source Definition

D3, D2, D1, D0	TCLK CONNECTION
0000	Tri-state TCLK
0001	Drive TCLK with TCLK 1
0010	Drive TCLK with TCLK 2
0011	Drive TCLK with TCLK 3
0100	Drive TCLK with TCLK 4
0101	Drive TCLK with TCLK 5
0110	Drive TCLK with TCLK 6
0111	Drive TCLK with TCLK 7
1000	Drive TCLK with TCLK 8
1010	Drive TCLK with T1 OSC
1011	Drive TCLK with E1 OSC
1100	Drive TCLK with 16.385MHz
1101	Drive TCLK with a logic 0
1110	Drive TCLK with a logic 1
1111	Tri-state TCLK

Note: Initial values are such that all ports are tri-stated.

Also note that RCLK from the LIU (DS21448) does not go directly to the FPGA. However, it is routed to the DS26401 and a test header. To get RCLK to fan out to all the ports on the DS26401, simply tri-state a port on the FPGA and manually jumper the RCLK X pin to the TCLK X pin. Then you can route that signal with register values 0001 to 1000 in the TCLK_SR.

Register Name: **RSYNC_SR**
Register Description: **DS26401 RSYNCx Pin Setting**
Register Offset: **0x0016, 0x0026, 0x0036, 0x0046, 0x0056, 0x0066, 0x0076, 0x0086**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x RSYNC Source (D3, D2, D1, D0)

The source for RSYNC is Defined as shown in Table 9.

Table 9. RSYNCx Source Definition

D3, D2, D1, D0	RSYNC CONNECTION
0000	Tri-state RSYNC
0001	Drive RSYNC with TSYNC 1
0010	Drive RSYNC with TSYNC 2
0011	Drive RSYNC with TSYNC 3
0100	Drive RSYNC with TSYNC 4
0101	Drive RSYNC with TSYNC 5
0110	Drive RSYNC with TSYNC 6
0111	Drive RSYNC with TSYNC 7
1000	Drive RSYNC with TSYNC 8
1010	Drive RSYNC with T1 OSC
1011	Drive RSYNC with E1 OSC
1100	Drive RSYNC with 16.385MHz
1101	Drive RSYNC with a logic 0
1110	Drive RSYNC with a logic 1
1111	Tri-state RSYNC

Note: Initial values are such that all ports are tri-stated.

Register Name: **TSYNC_SR**
Register Description: **DS26401 TSYNCx Pin Setting**
Register Offset: **0x0017, 0x0027, 0x0037, 0x0047, 0x0057, 0x0067, 0x0077, 0x0087**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	D4	D3	D2	D1	D0

Bit 0 to 2: DS26401 Port x TSYNC Source (D4, D3, D2, D1, D0)

The source for TSYNC is Defined as shown in Table 10.

Table 10. TSYNCx Source Definition

D4, D3, D2, D1, D0	TSYNC CONNECTION
00000	Tri-state TSYNC
00001	Drive TSYNC with RSYNC 1
00010	Drive TSYNC with RSYNC 2
00011	Drive TSYNC with RSYNC 3
00100	Drive TSYNC with RSYNC 4
00101	Drive TSYNC with RSYNC 5
00110	Drive TSYNC with RSYNC 6
00111	Drive TSYNC with RSYNC 7
01000	Drive TSYNC with RSYNC 8
01010	Drive TSYNC with T1 OSC
01011	Drive TSYNC with E1 OSC
01100	Drive TSYNC with 16.385MHz
01101	Drive TSYNC with a logic 0
01110	Drive TSYNC with a logic 1
10001	Drive TSYNC with RMSYNC 1
10010	Drive TSYNC with RMSYNC 2
10011	Drive TSYNC with RMSYNC 3
10100	Drive TSYNC with RMSYNC 4
10101	Drive TSYNC with RMSYNC 5
10110	Drive TSYNC with RMSYNC 6
10111	Drive TSYNC with RMSYNC 7
11000	Drive TSYNC with RMSYNC 8
11111	Tri-state TSYNC

Note: Initial values are such that all ports are tri-stated.

Register Name: **CLK_SR**
Register Description: **DS21448 MCLK A, DS21448 MCLK B, and REF CLK**
Register Offset: **0x0090**

Bit #	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Table 11. MCLK A Source Definition

D1, D0	MCLK A (DS21448 PORTS 1 TO 4)
00	Tri-state MCLK
01	Drive MCLK with 1.544MHz
10	Drive MCLK with 2.048MHz
11	Tri-state MCLK

Note: Initial values are such that MCLK is 2.048MHz.

Table 12. MCLK B Source Definition

D3, D2	MCLK B (DS21448 PORTS 5 TO 8)
00	Tri-state MCLK
01	Drive MCLK with 1.544MHz
10	Drive MCLK with 2.048MHz
11	Tri-state MCLK

Note: Initial values are such that that MCLK is 2.048MHz.

Table 13. MCLK A Source Definition

D5, D4	REF CLK
00	Tri-state REF CLK
01	Drive REF with 1.544MHz
10	Drive REF with 2.048MHz
11	Tri-state REF CLK

Note: Initial values are such that REF is 2.048MHz.

DS26401 AND DS21448 INFORMATION

For more information about the DS26401 and DS21448, please consult the respective data sheets, available on our website at www.maxim-ic.com/DS26401 and www.maxim-ic.com/DS21448.

TECHNICAL SUPPORT

For technical support, please email your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS26401DK schematics are featured in the following pages.

CR-1 : @DS26401DK01A0_LIB.DS26401DK01A0DN<SCH_1>:PAGE1

DS26401 DESIGN KIT

CREATED BY

ROBERT E. SPENCER

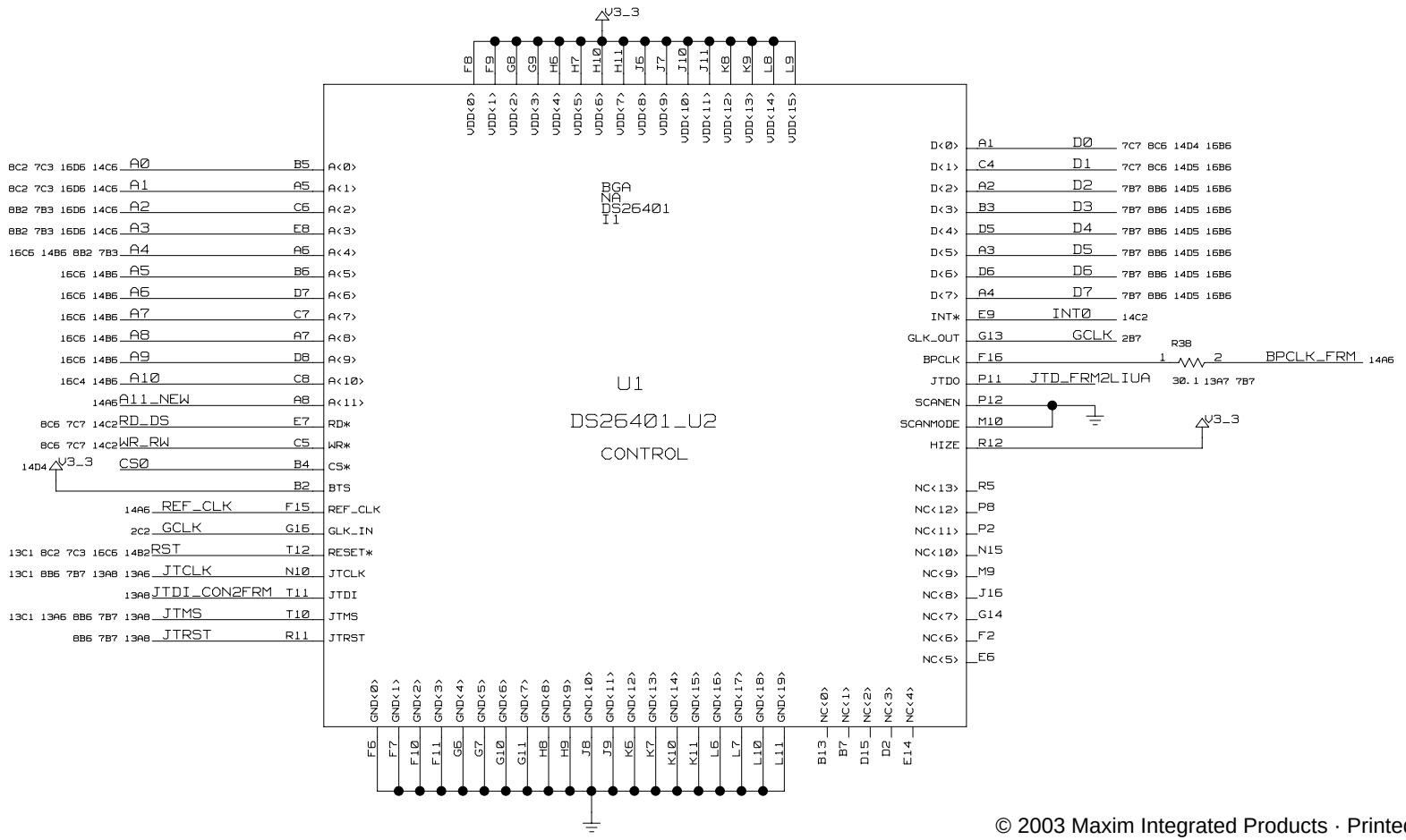
JUNE 3, 2003

DALLAS SEMICONDUCTOR / MAXIM

Mon Jul 21 13:41:48 2003

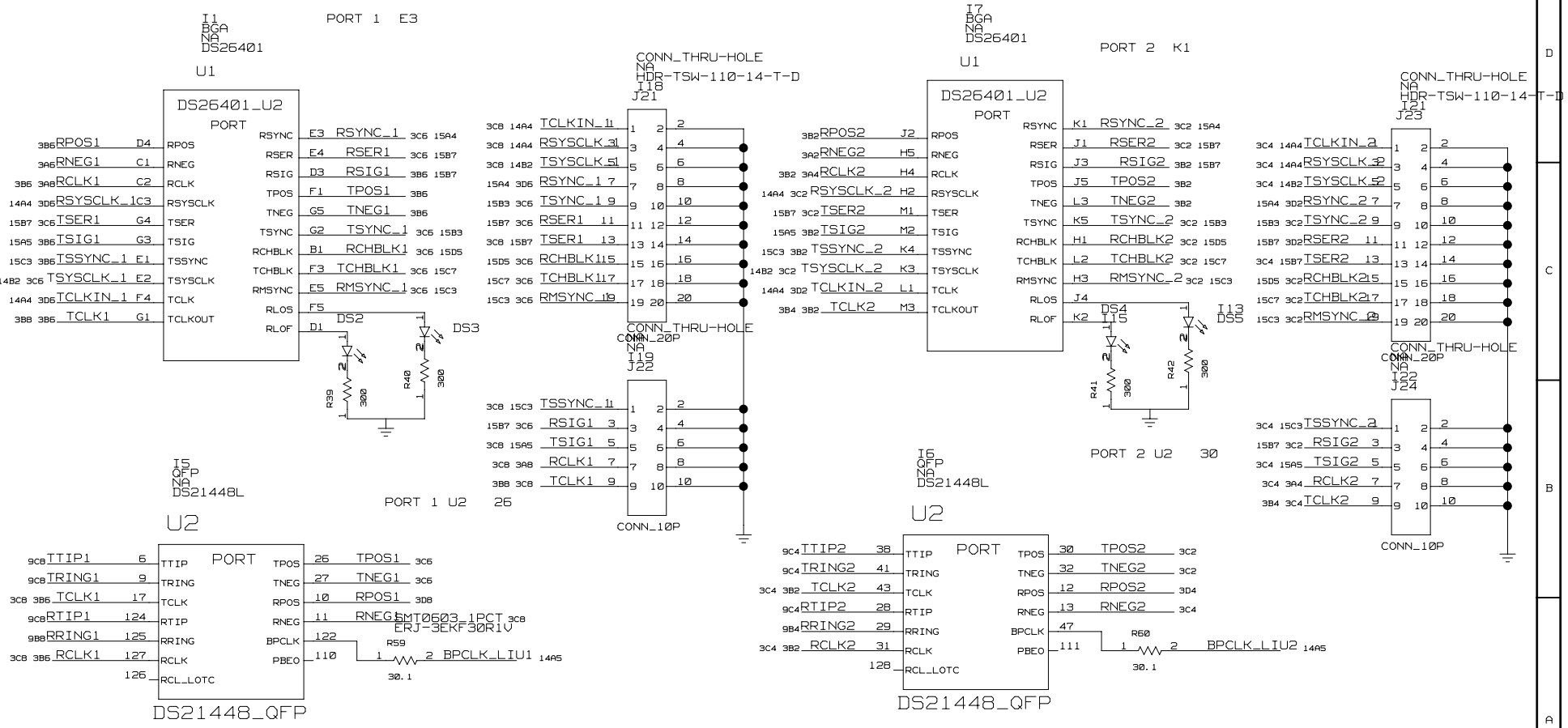
TITLE: DS26401 DESIGN KIT TITLE PAGE	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 1

CR-2 : @DS26401DK01A0_LIB.DS26401DK01A0DN<SCH_1>:PAGE2



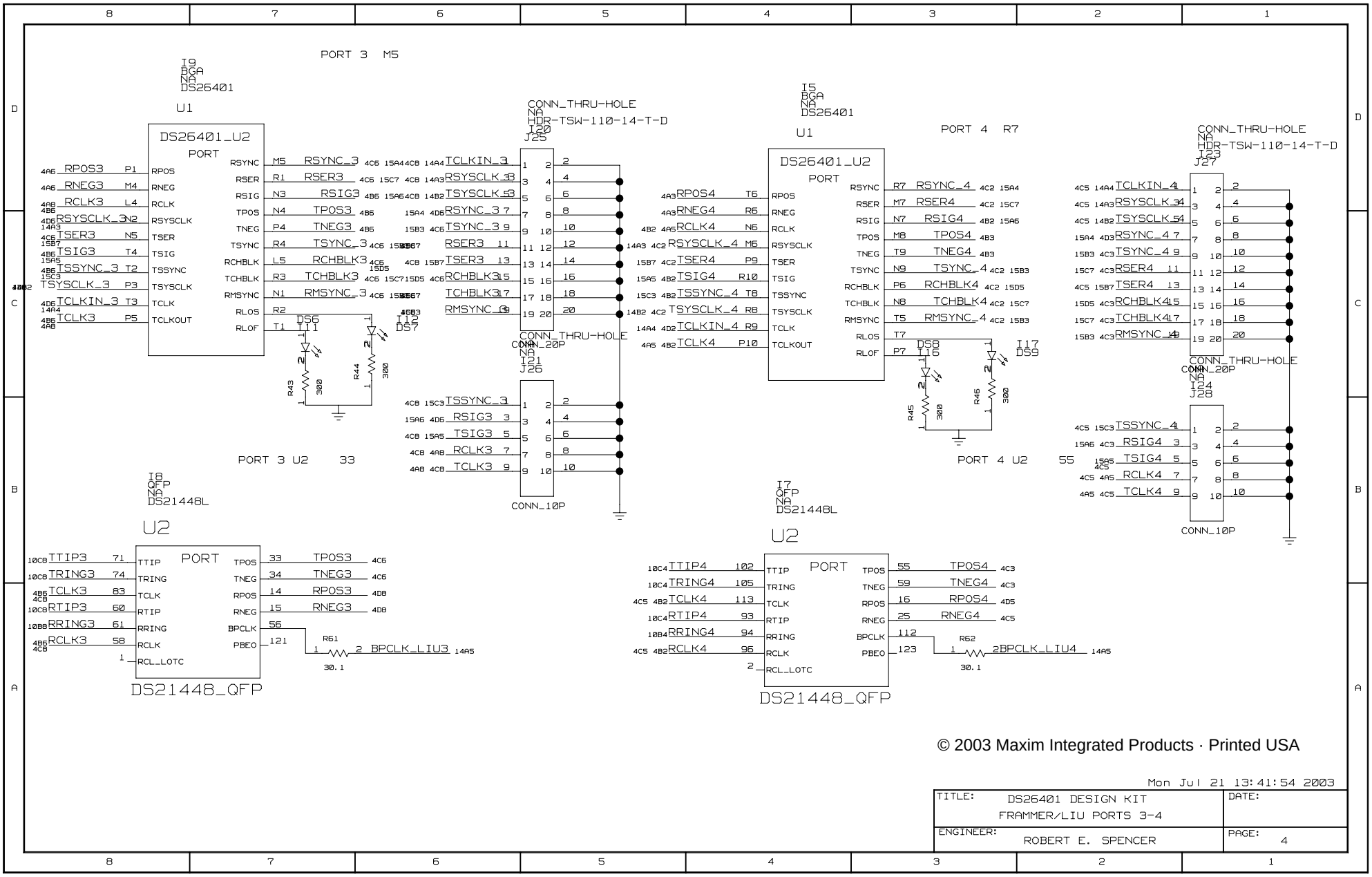
Mon Jul 21 13:41:52 2003

TITLE: DS26401 DESIGN KIT DS26401 CONTROL BLOCK	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 2



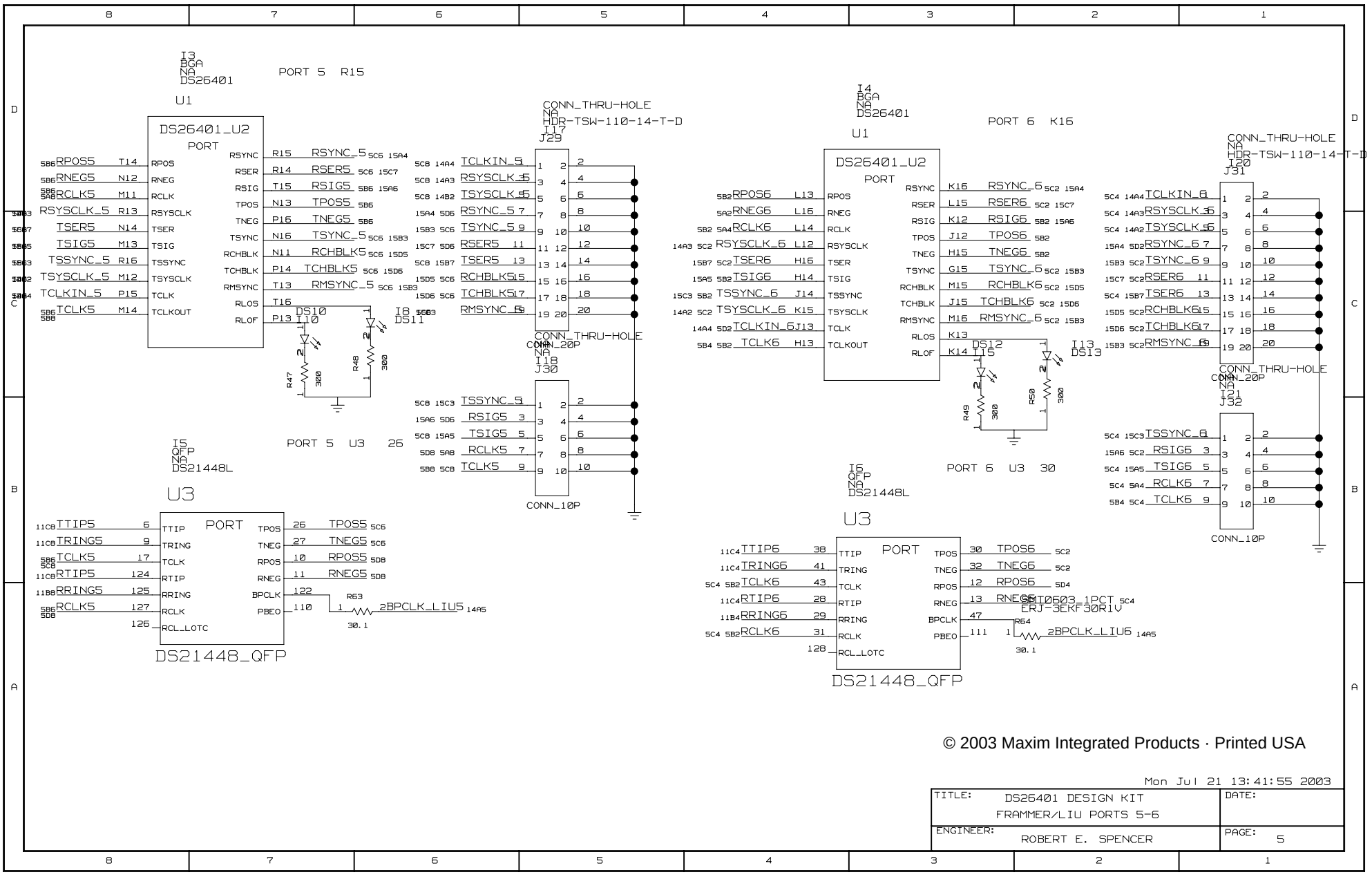
Mon Jul 21 13:41:52 2003

TITLE: DS26401 DESIGN KIT FRAMMER/LIU PORTS 1-2	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 3



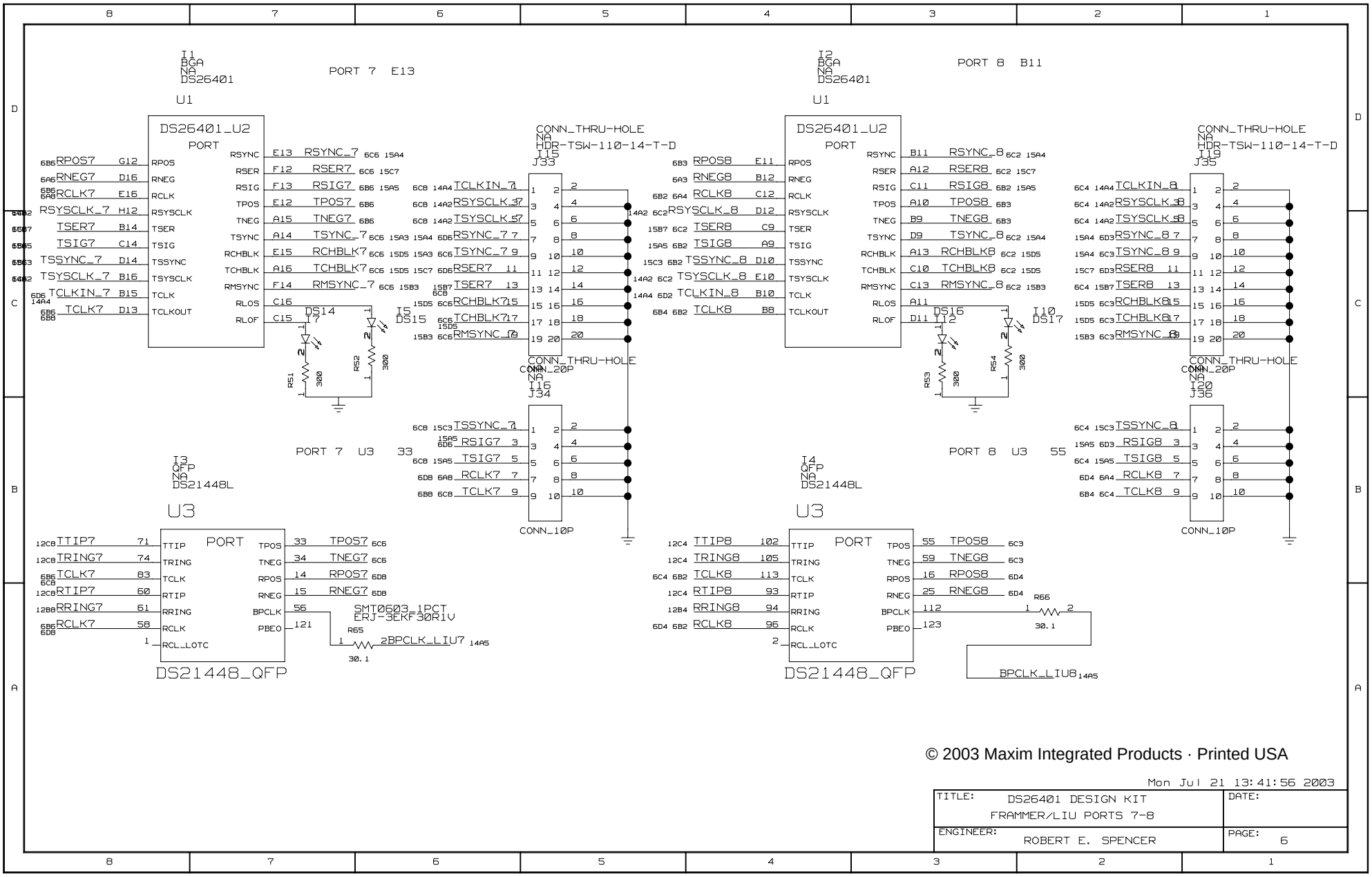
Mon Jul 21 13:41:54 2003

TITLE: DS26401 DESIGN KIT FRAMMER/LIU PORTS 3-4	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 4



Mon Jul 21 13:41:55 2003

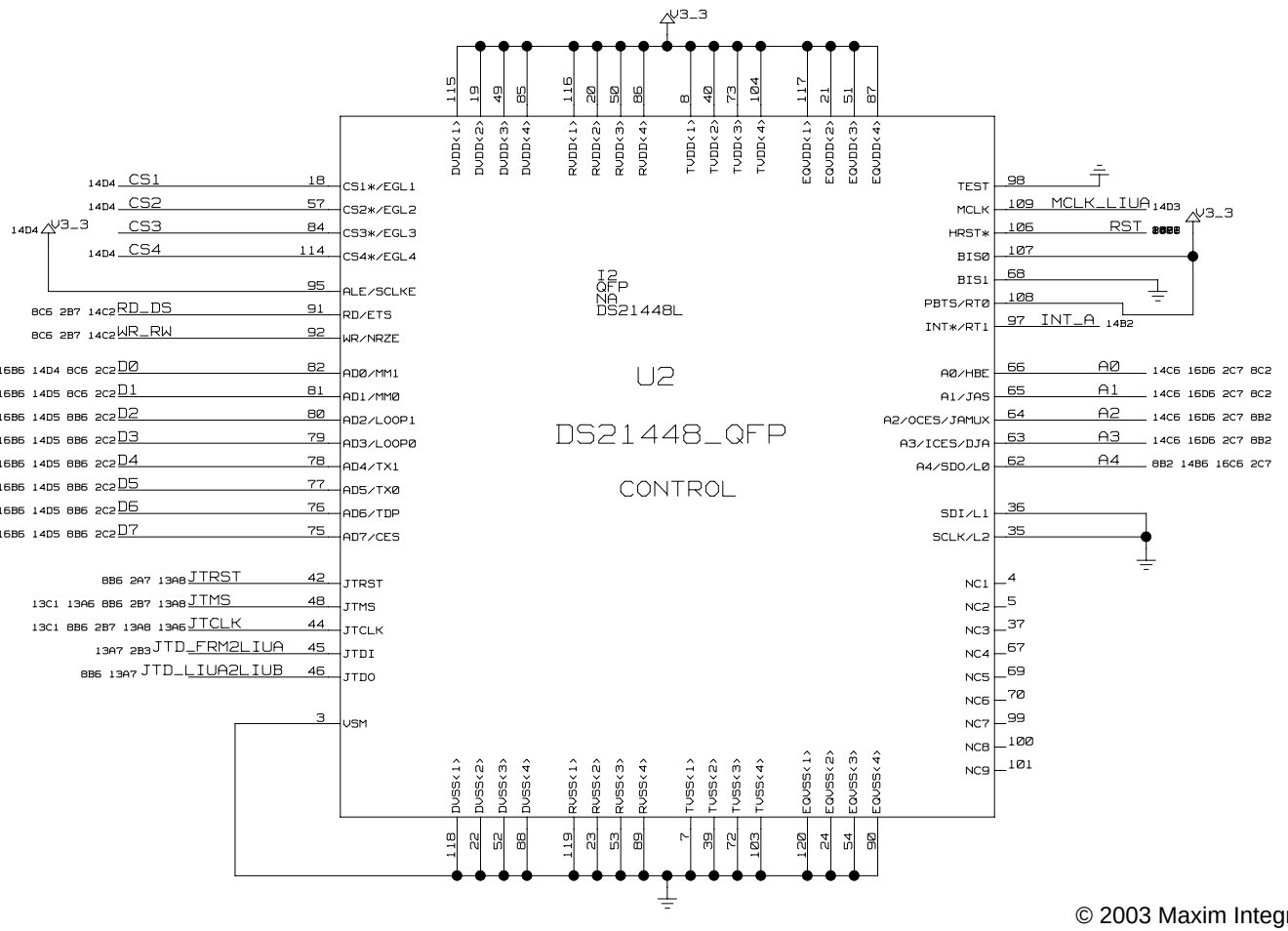
TITLE: DS26401 DESIGN KIT FRAMMER/LIU PORTS 5-6	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 5



Mon Jul 21 13:41:56 2003

TITLE: DS26401 DESIGN KIT FRAMMER/LIU PORTS 7-8	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 6

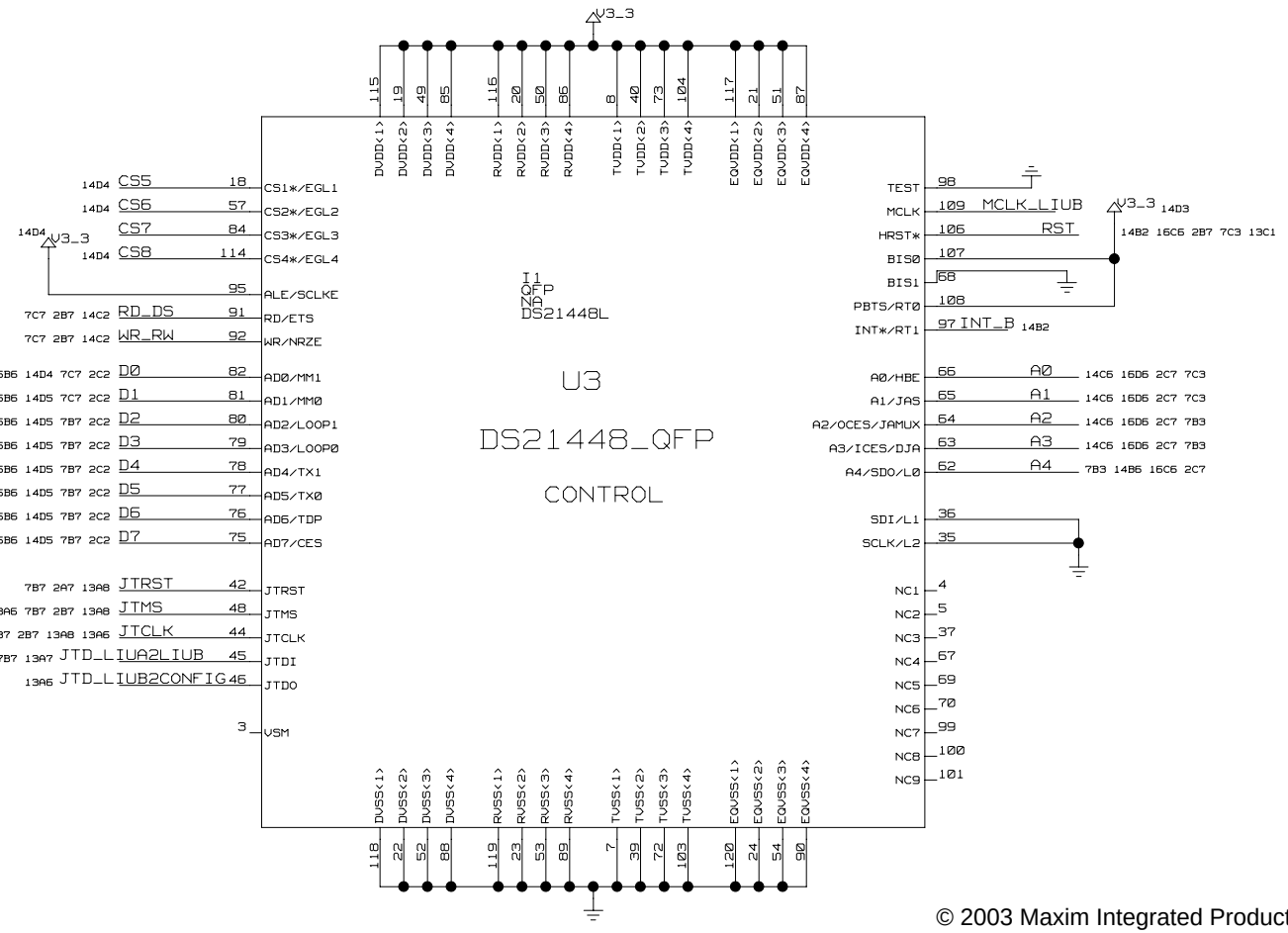
CR-7 : @DS26401DK01A0_LIB.DS26401DK01A0DN(SCH_1):PAGE7



Mon Jul 21 13:41:58 2003

TITLE: DS26401 DESIGN KIT LIU CONTROL PORT 1-4	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 7

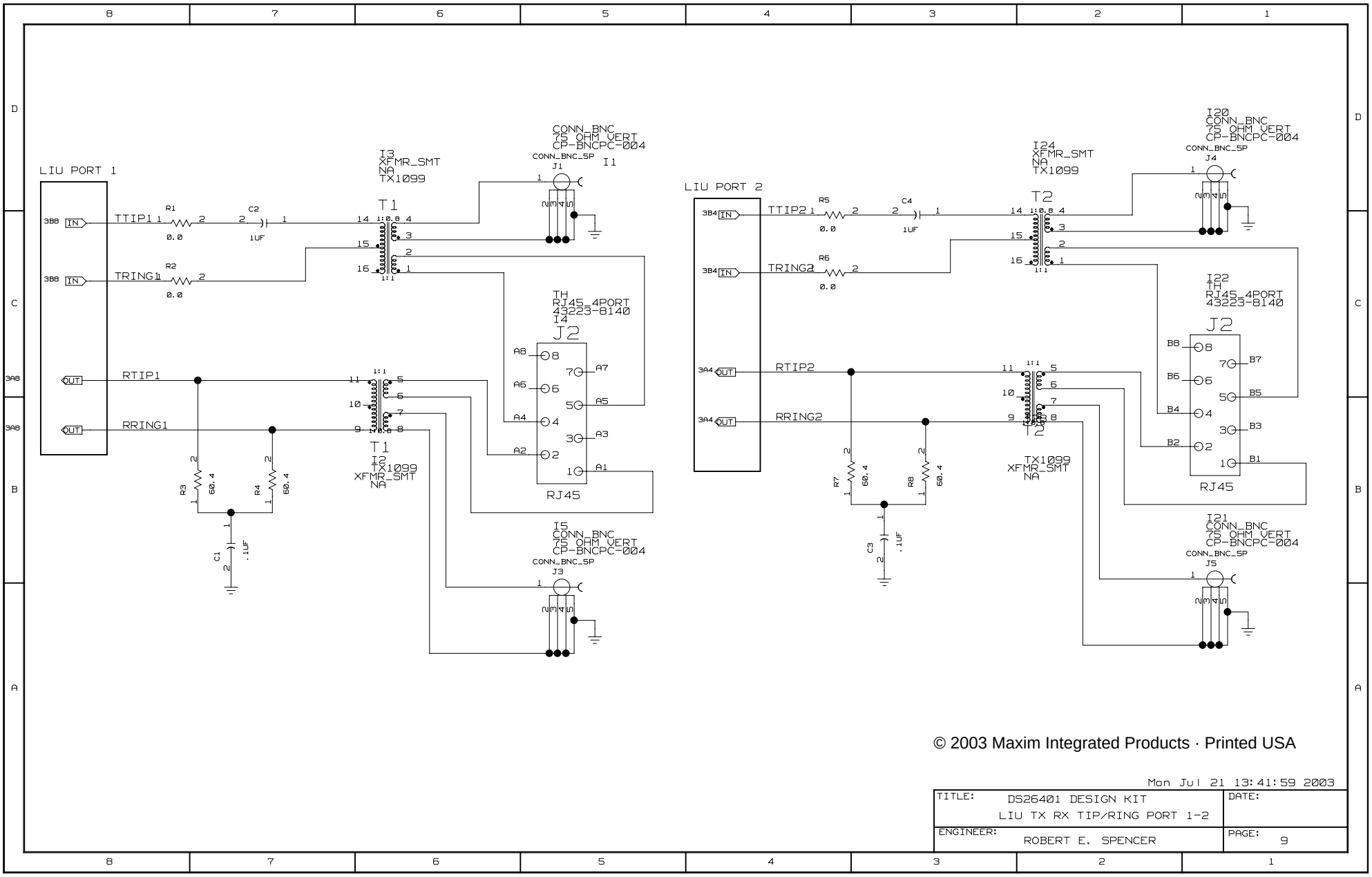
CR-8 : @DS26401DK01A0_LIB.DS26401DK01A0DN(SCH_1):PAGE8



Mon Jul 21 13:41:59 2003

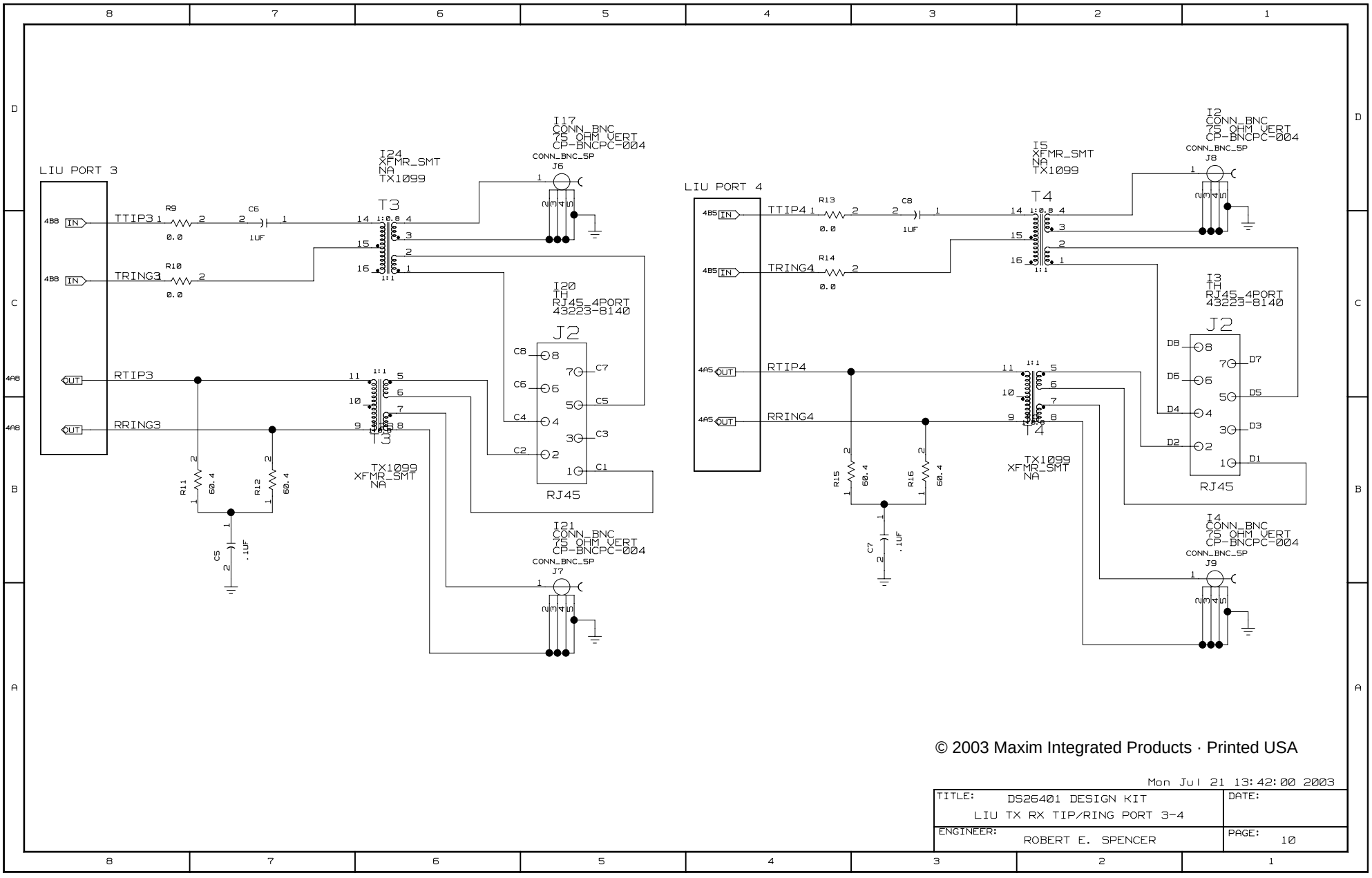
TITLE: DS26401 DESIGN KIT LIU CONTROL PORT 5-8	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 8

CR-9 : @DS26401DK01A0_LIB.DS26401DK01A0DN(SCH_1):PAGE9



Mon Jul 21 13:41:59 2003

TITLE: DS26401 DESIGN KIT LIU TX RX TIP/RING PORT 1-2	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 9


LIU PORT 3
TTIP3
TRING3
RTIP3
RRING3
R9
R10
R11
R12
C5
C6
T3
I24
XFMR_SMT
NA
TX1099
I17
CONN_BNC
75 OHM VERT
CP-BNCPC-004
CONN_BNC_5P
J6
I20
TH
RJ45_4PORT
43223-8140
J2
RJ45
I21
J7
LIU PORT 4
TTIP4
TRING4
RTIP4
RRING4
R13
R14
R15
R16
C7
C8
T4
I5
I2
J8
I3
I4
J9
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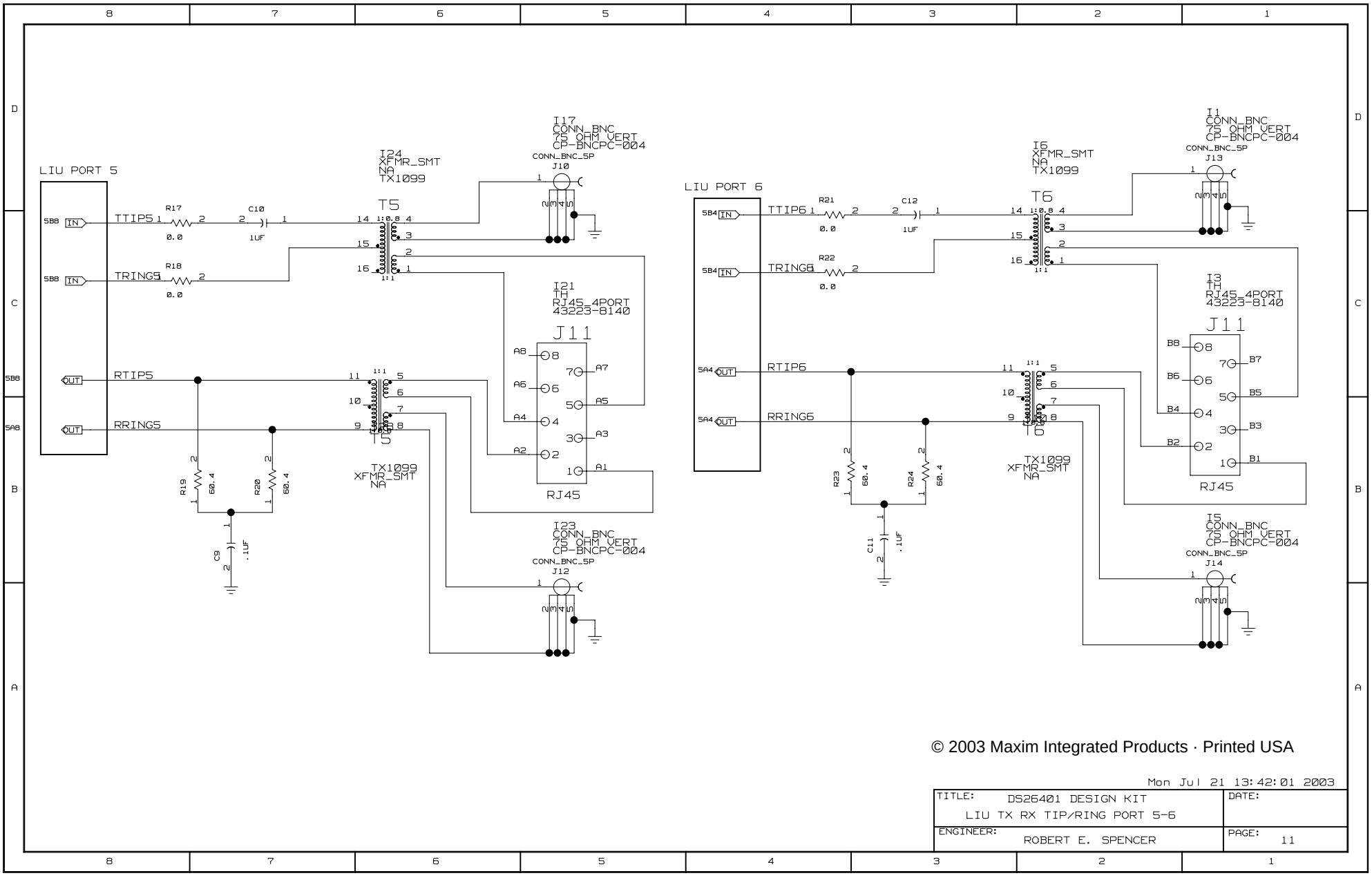
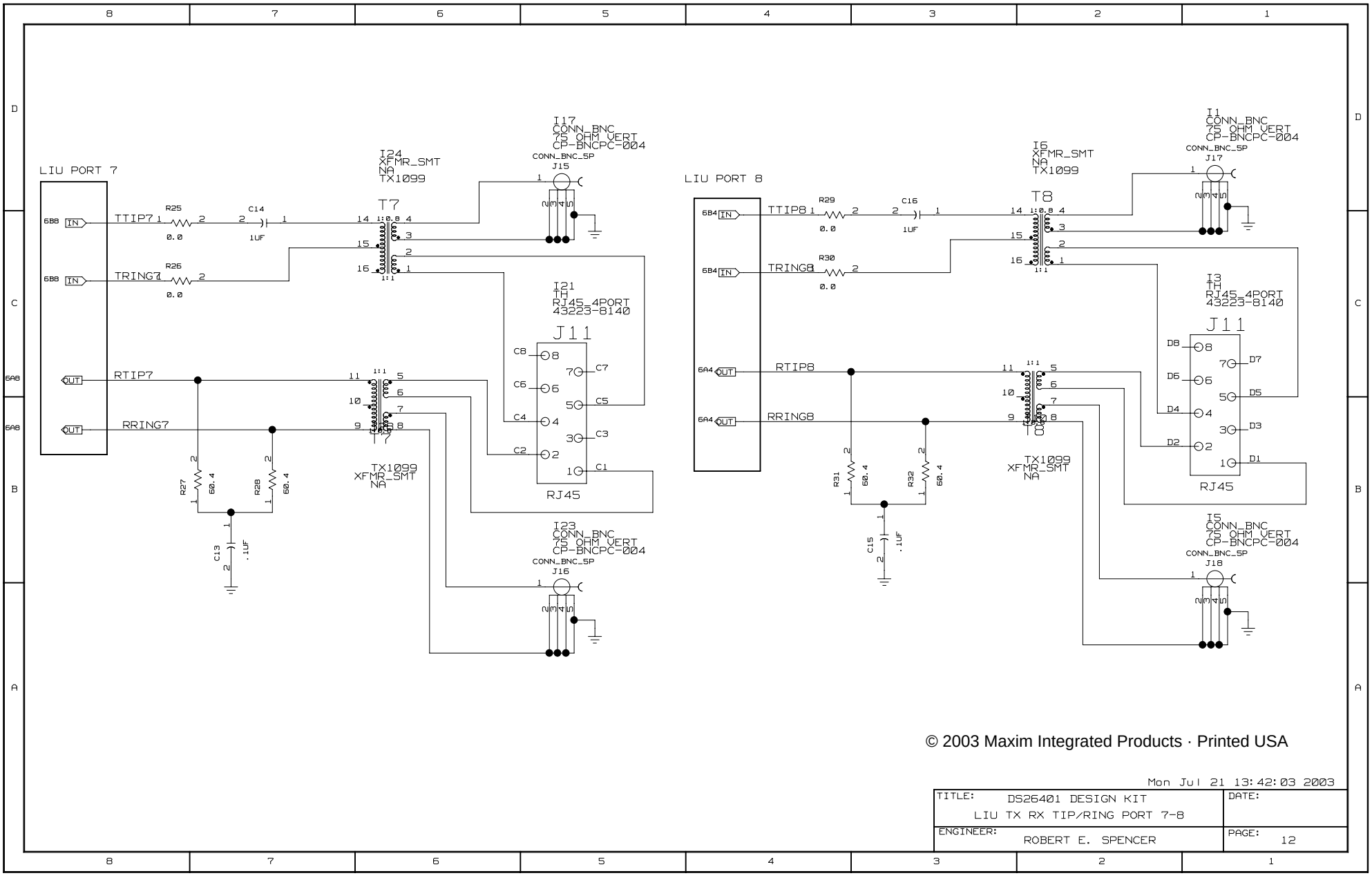
Mon Jul 21 13:42:00 2003
TITLE: DS26401 DESIGN KIT
LIU TX RX TIP/RING PORT 3-4
DATE:
ENGINEER: ROBERT E. SPENCER
PAGE: 10


LIU PORT 5
TTIP5
TRING5
RTIP5
RRING5
R17
R18
R19
R20
C10
C9
T5
T4
I24
XFMR_SMT
NA
TX1099
I17
CONN_BNC
75 OHM VERT
CP-BNCPC-004
CONN_BNC_5P
J10
I21
TH
RJ45_4PORT
43223-8140
J11
RJ45
I23
J12
LIU PORT 6
TTIP6
TRING6
RTIP6
RRING6
R21
R22
R23
R24
C12
C11
T6
T7
I6
I1
J13
I3
I5
J14
© 2003 Maxim Integrated Products · Printed USA
Mon Jul 21 13:42:01 2003
TITLE: DS26401 DESIGN KIT
LIU TX RX TIP/RING PORT 5-6
DATE:
ENGINEER: ROBERT E. SPENCER
PAGE: 11


LIU PORT 7
TTIP7
TRING7
RTIP7
RRING7
R25
R26
R27
R28
C13
C14
T7
I24
XFMR_SMT
NA
TX1099
I17
CONN_BNC
75 OHM VERT
CP-BNCPC-004
CONN_BNC_5P
J15
J16
I21
TH
RJ45_4PORT
43223-8140
J11
RJ45
I23
LIU PORT 8
TTIP8
TRING8
RTIP8
RRING8
R29
R30
R31
R32
C15
C16
T8
I6
I1
J17
I3
I5
J18
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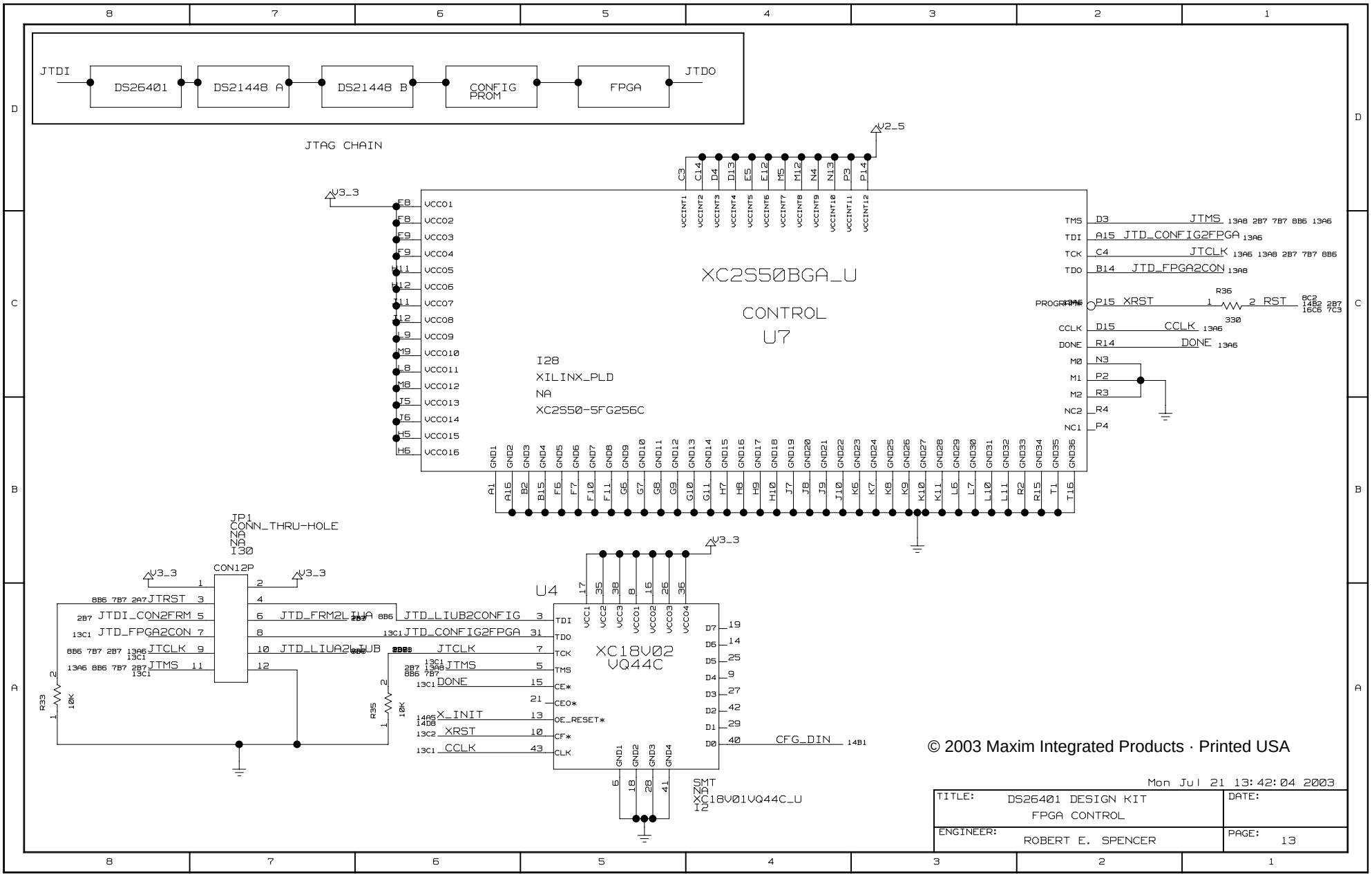
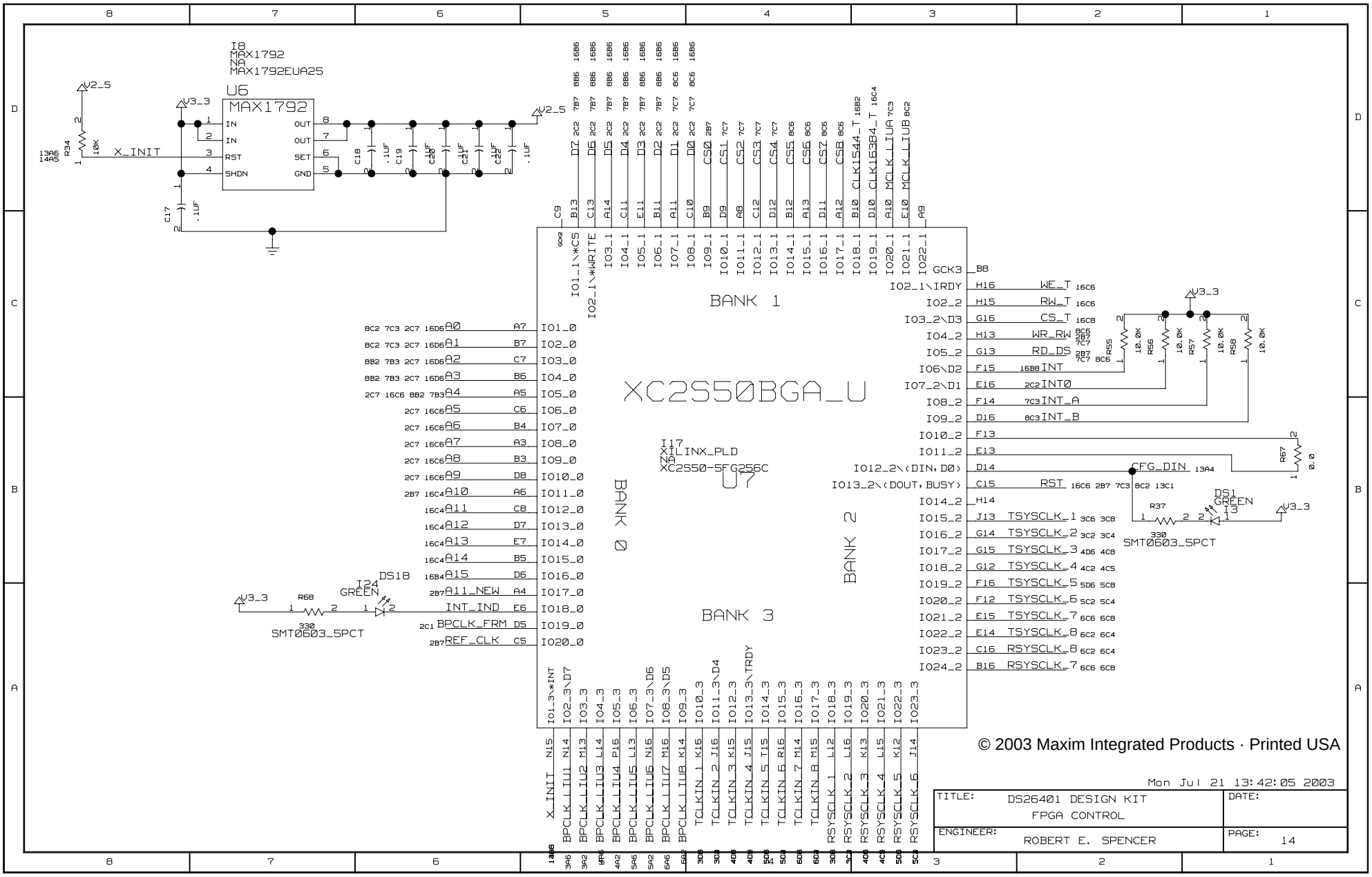
Mon Jul 21 13:42:03 2003
TITLE: DS26401 DESIGN KIT
LIU TX RX TIP/RING PORT 7-8
DATE:
ENGINEER: ROBERT E. SPENCER
PAGE: 12



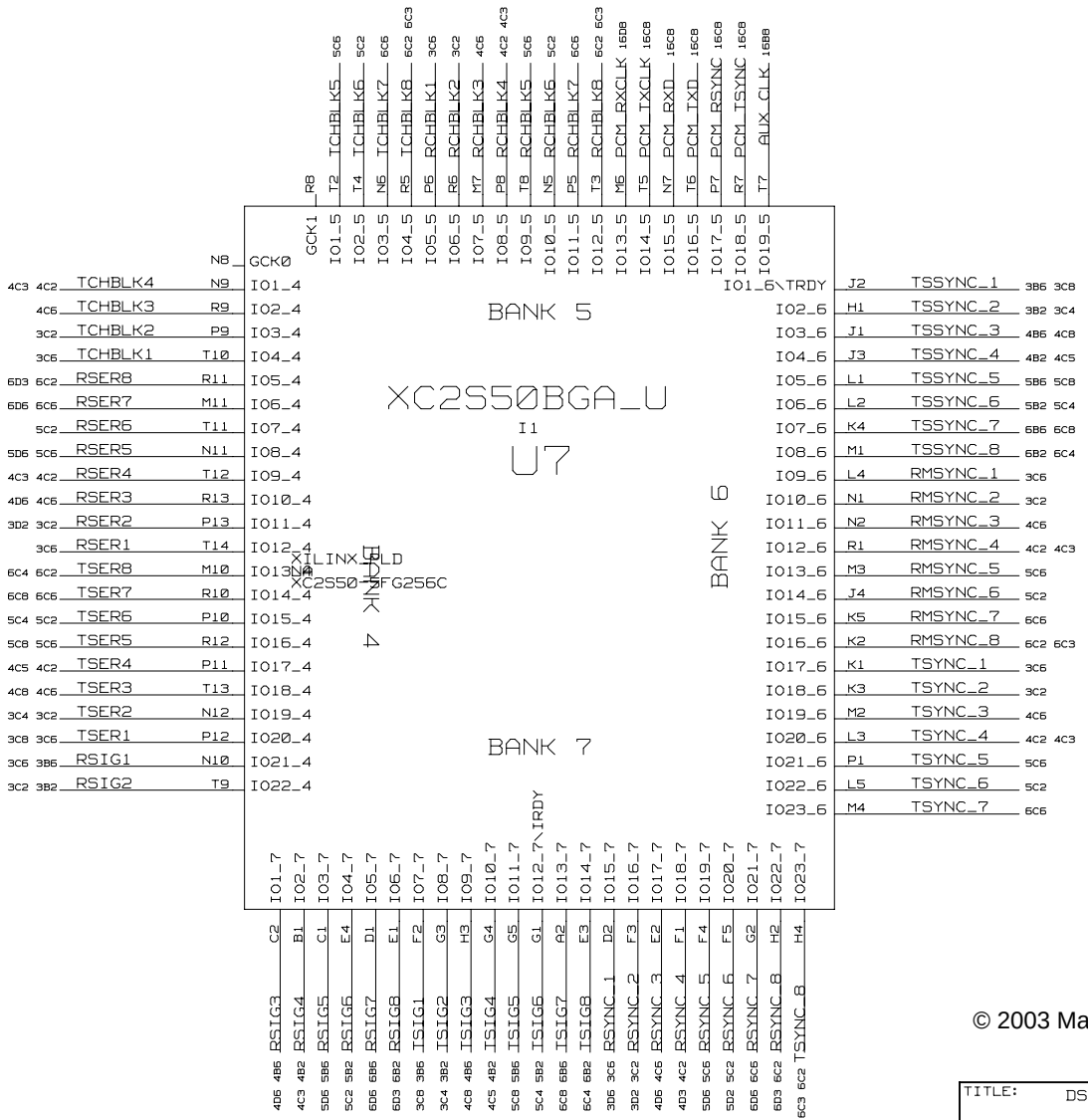
Mon Jul 21 13:42:04 2003

TITLE: DS26401 DESIGN KIT FPGA CONTROL	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 13



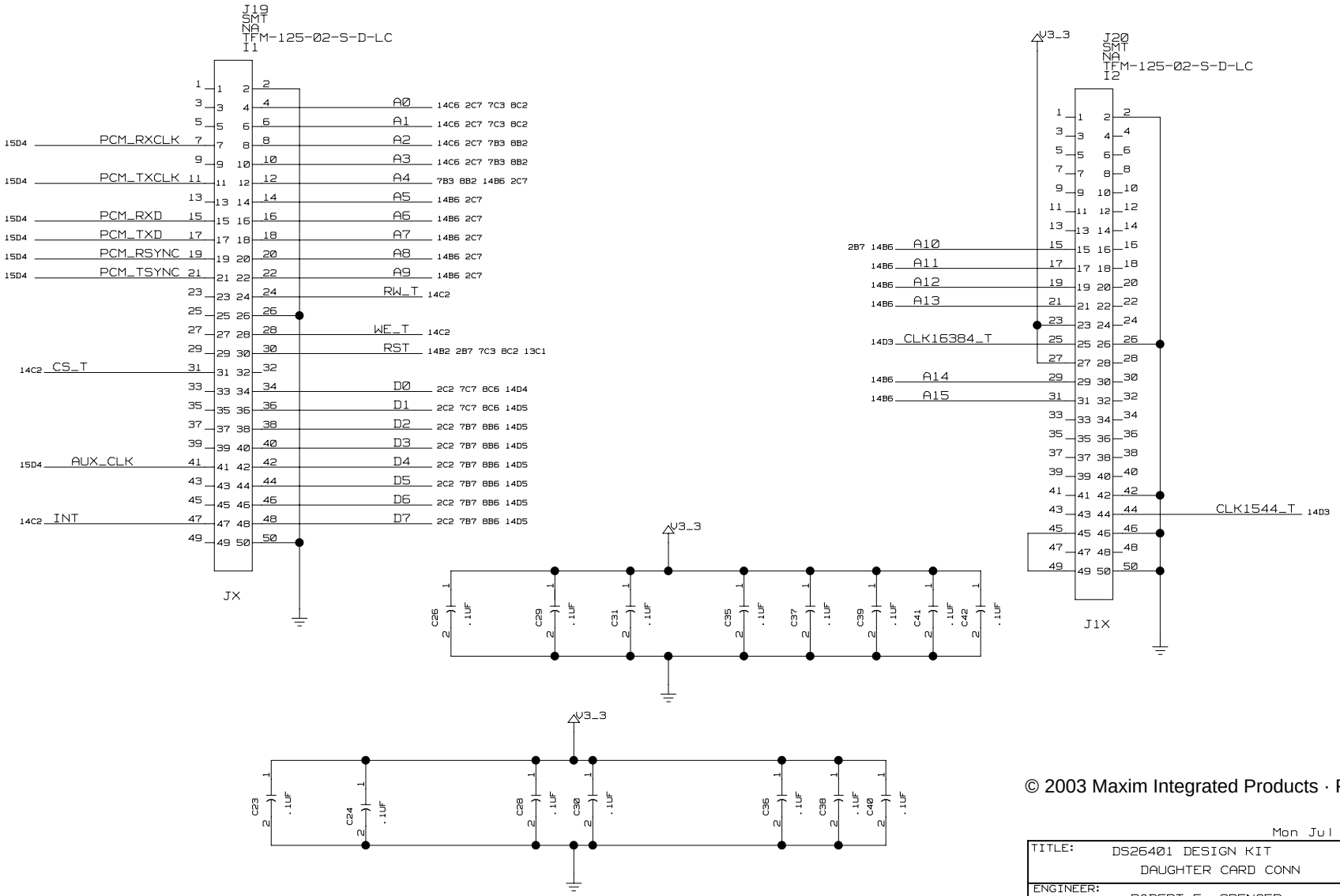
Mon Jul 21 13:42:05 2003

TITLE: DS26401 DESIGN KIT FPGA CONTROL	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 14



Mon Jul 21 13:42:06 2003

TITLE: DS26401 DESIGN KIT FPGA CONTROL	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 15



Mon Jul 21 13:42:07 2003

TITLE: DS26401 DESIGN KIT DAUGHTER CARD CONN	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 16

CR-17 : @DS26401DK01A0_LIB.DS26401DK01A0DN(SCH_1):PAGE17

Mon Jul 21 13:42:08 2003

TITLE: DS26401 DESIGN KIT FPGA CONTROL	DATE:
ENGINEER: ROBERT E. SPENCER	PAGE: 17

*** Signal Cross-Reference for the entire design ***

A0	14C6< > 16D6< > 2C7< 7C3< 8C2<
A1	14C6< > 16D6< > 2C7< 7C3< 8C2<
A2	14C6< > 16D6< > 2C7< 7B3< 8B2<
A3	14C6< > 16D6< > 2C7< 7B3< 8B2<
A4	7B3< > 8B2< > 14B6< > 16C6< > 2C7<
A5	14B6< > 16C6< > 2C7<
A6	14B6< > 16C6< > 2C7<
A7	14B6< > 16C6< > 2C7<
A8	14B6< > 16C6< > 2C7<
A9	14B6< > 16C6< > 2C7<
A10	14B6< > 16C4< > 2B7<
A11	14B6< > 16C4< >
A11_NEW	14A6< > 2B7<
A12	14B6< > 16C4< >
A13	14B6< > 16C4< >
A14	14B6< > 16C4< >
A15	14B6< > 16B4< >
AUX_CLK	15D4< > 16B8< >
BPCLK_FRM	14A6< > 2C1<
BPCLK_LIU1	14A5< > 3A6<
BPCLK_LIU2	14A5< > 3A2<
BPCLK_LIU3	14A5< > 4A6<
BPCLK_LIU4	14A5< > 4A2<
BPCLK_LIU5	14A5< > 5A6<
BPCLK_LIU6	14A5< > 5A2<
BPCLK_LIU7	14A5< > 6A6<
BPCLK_LIU8	14A5< > 6A2<
CCLK	13A6< 13C1<
CFG_DIN	13A4> 14B1< >
CLK1544_T	14D3< > 16B2< >
CLK16384_T	14D3< > 16C4< >
CS0	14D4< > 2B7<
CS1	14D4< > 7C7<
CS2	14D4< > 7C7<
CS3	14D4< > 7C7<
CS4	14D4< > 7C7<
CS5	14D4< > 8C6<
CS6	14D4< > 8C6<
CS7	14D4< > 8C6<
CS8	14D4< > 8C6<
CS_T	14C2< > 16C8< >
D0	2C2< > 7C7< > 8C6< > 14D4< > 16B6< >
D1	2C2< > 7C7< > 8C6< > 14D5< > 16B6< >
D2	2C2< > 7B7< > 8B6< > 14D5< > 16B6< >
D3	2C2< > 7B7< > 8B6< > 14D5< > 16B6< >
D4	2C2< > 7B7< > 8B6< > 14D5< > 16B6< >
D5	2C2< > 7B7< > 8B6< > 14D5< > 16B6< >
D6	2C2< > 7B7< > 8B6< > 14D5< > 16B6< >
D7	2C2< > 7B7< > 8B6< > 14D5< > 16B6< >
DONE	13A6< 13C1<
GCLK	2C2> 2B7<
INT	14C2< > 16B8< >
INT0	2C2> 14C2< >
INT_A	7C3< > 14B2< >
INT_B	8C3< > 14B2< >
INT_IND	14A6< >
JTCLK	13A6< > 13A8< > 2B7< 7B7< 8B6< 13C1<
JTDI_CON2FRM	13A8< > 2B7<
JTD_CONFIG2FPGA	13A6< > 13C1<
JTD_FPGA2CON	13A8< > 13C1>
JTD_FRM2LIUA	2B3> 13A7< > 7B7<
JTD_LIUA2LIUB	13A7< > 7B7< 8B6<
JTD_LIUB2CONFIG	13A6< > 8B6<
JTMS	13A8< > 2B7< 7B7< 8B6< 13A6< 13C1<
JTRST	13A8< > 2A7< 7B7< 8B6<
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MCLK_LIUB	14D3< > 8C2<
PCM_RSYNC	15D4< > 16C8< >
PCM_RXCLK	15D4< > 16D8< >
PCM_RXD	15D4< > 16C8< >
PCM_TSYNC	15D4< > 16C8< >
PCM_TXCLK	15D4< > 16C8< >
PCM_TXD	15D4< > 16C8< >
RCHBLK1	3C6> 3C6< > 15D5< >
RCHBLK2	3C2> 3C2< > 15D5< >
RCHBLK3	4C6< > 4C6> 15D5< >
RCHBLK4	4C2< > 4C3> 15D5< >
RCHBLK5	5C6< > 5C6> 15D5< >
RCHBLK6	5C2< > 5C2> 15D5< >
RCHBLK7	6C6< > 6C6> 15D5< >
RCHBLK8	6C2< > 6C3> 15D5< >
RCLK1	3A8> 3B6< > 3C8<
RCLK2	3A4> 3B2< > 3C4<
RCLK3	4A8> 4B6< > 4C8<
RCLK4	4A5> 4B2< > 4C5<
RCLK5	5A8> 5B6< > 5D8<
RCLK6	5A4> 5B2< > 5C4<
RCLK7	6A8> 6B6< > 6D8<
RCLK8	6A4> 6B2< > 6D4<
RD_DS	14C2< > 2B7< 7C7< 8C6<
REF_CLK	14A6< > 2B7<
RMSYNC_1	3C6> 3C6< > 15C3< >
RMSYNC_2	3C2> 3C2< > 15C3< >
RMSYNC_3	4C6< > 4C6> 15B3< >
RMSYNC_4	4C2< > 4C3> 15B3< >
RMSYNC_5	5C6< > 5C6> 15B3< >
RMSYNC_6	5C2< > 5C2> 15B3< >
RMSYNC_7	6C6< > 6C6> 15B3< >
RMSYNC_8	6C2< > 6C3> 15B3< >
RNEG1	3A6> 3C8<
RNEG2	3A2> 3C4<
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RNEG7	6A6> 6D8<
RNEG8	6A3> 6D4<
RPOS1	3B6> 3D8<
RPOS2	3B2> 3D4<
RPOS3	4A6> 4D8<
RPOS4	4A3> 4D5<
RPOS5	5B6> 5D8<
RPOS6	5B2> 5D4<
RPOS7	6B6> 6D8<
RPOS8	6B3> 6D4<
RRING1	9B8> 3A8<
RRING2	9B4> 3A4<
RRING3	10B8> 4A8<
RRING4	10B4> 4A5<
RRING5	11B8> 5A8<
RRING6	11B4> 5A4<
RRING7	12B8> 6A8<
RRING8	12B4> 6A4<
RSER1	3C6> 3C6< > 15B7< >
RSER2	3C2< > 3D2> 15B7< >
RSER3	4C6< > 4D6> 15C7< >
RSER4	4C2< > 4C3> 15C7< >
RSER5	5C6< > 5D6> 15C7< >
RSER6	5C2< > 5C2> 15C7< >
RSER7	6C6< > 6D6> 15C7< >
RSER8	6C2< > 6D3> 15C7< >
RSIG1	3B6< > 3C6> 15B7< >
RSIG2	3B2< > 3C2> 15B7< >
RSIG3	4B6< > 4D6> 15A6< >
RSIG4	4B2< > 4C3> 15A6< >
RSIG5	5B6< > 5D6> 15A6< >
RSIG6	5B2< > 5C2> 15A6< >
RSIG7	6B6< > 6D6> 15A5< >
RSIG8	6B2< > 6D3> 15A5< >
RST	14B2< > 16C6< > 2B7< 7C3< 8C2< 13C1<
RSYNC_1	3C6< > 3D6< > 15A4< >
RSYNC_2	3C2< > 3D2< > 15A4< >
RSYNC_3	4C6< > 4D6< > 15A4< >
RSYNC_4	4C2< > 4D3< > 15A4< >
RSYNC_5	5C6< > 5D6< > 15A4< >
RSYNC_6	5C2< > 5D2< > 15A4< >
RSYNC_7	6C6< > 6D6< > 15A4< >
RSYNC_8	6C2< > 6D3< > 15A4< >
RSYSCLK_1	3D6< > 14A4< > 3C8<
RSYSCLK_2	3C2< > 14A4< > 3C4<
RSYSCLK_3	4D6< > 14A3< > 4C8<
RSYSCLK_4	4C2< > 14A3< > 4C5<
RSYSCLK_5	5D6< > 14A3< > 5C8<
RSYSCLK_6	5C2< > 14A3< > 5C4<
RSYSCLK_7	6C6< > 14A2< > 6C8<
RSYSCLK_8	6C2< > 14A2< > 6C4<
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RTIP3	10C8> 4A8<
RTIP4	10C4> 4A5<
RTIP5	11C8> 5B8<
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RTIP7	12C8> 6A8<
RTIP8	12C4> 6A4<
RW_T	14C2< > 16C6< >
TCHBLK1	3C6> 3C6< > 15C7< >
TCHBLK2	3C2> 3C2< > 15C7< >
TCHBLK3	4C6< > 4C6> 15C7< >
TCHBLK4	4C2< > 4C3> 15C7< >
TCHBLK5	5C6< > 5C6> 15D6< >
TCHBLK6	5C2< > 5C2> 15D6< >
TCHBLK7	6C6< > 6C6> 15D5< >
TCHBLK8	6C2< > 6C3> 15D5< >
TCLK1	3B6< > 3C8> 3B8<
TCLK2	3B2< > 3C4> 3B4<
TCLK3	4B6< > 4C8> 4A8<
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TNEG3	4C6> 4B6<
TNEG4	4C3> 4B3<
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TRING7	6B8> 12C8<
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TSER1	3C6< > 15B7< > 3C8<
TSER2	3C2< > 15B7< > 3C4<
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TSER4	4C2< > 15B7< > 4C5<
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TSER6	5C2< > 15B7< > 5C4<
TSER7	6C6< > 15B7< > 6C8<
TSER8	6C2< > 15B7< > 6C4<
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TSIG2	3B2< > 15A5< > 3C4<
TSIG3	4B6< > 15A5< > 4C8<
TSIG4	4B2< > 15A5< > 4C5<
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TSSYNC_3	4B6< > 15C3< > 4C8<
TSSYNC_4	4B2< > 15C3< > 4C5<
TSSYNC_5	5B6< > 15C3< > 5C8<
TSSYNC_6	5B2< > 15C3< > 5C4<
TSSYNC_7	6B6< > 15C3< > 6C8<
TSSYNC_8	6B2< > 15C3< > 6C4<
TSYNC_1	3C6< > 3C6< > 15B3< >
TSYNC_2	3C2< > 3C2< > 15B3< >
TSYNC_3	4C6< > 4C6< > 15B3< >
TSYNC_4	4C2< > 4C3< > 15B3< >
TSYNC_5	5C6< > 5C6< > 15B3< >
TSYNC_6	5C2< > 5C2< > 15B3< >
TSYNC_7	6C6< > 6C6< > 15A3< >
TSYNC_8	6C2< > 6C3< > 15A4< >
TSYSCLK_1	3C6< > 14B2< > 3C8<
TSYSCLK_2	3C2< > 14B2< > 3C4<
TSYSCLK_3	4D6< > 14B2< > 4C8<
TSYSCLK_4	4C2< > 14B2< > 4C5<
TSYSCLK_5	5D6< > 14B2< > 5C8<
TSYSCLK_6	5C2< > 14A2< > 5C4<
TSYSCLK_7	6C6< > 14A2< > 6C8<
TSYSCLK_8	6C2< > 14A2< > 6C4<
TTIP1	3B8> 9C8<
TTIP2	3B4> 9C4<
TTIP3	4B8> 10C8<
TTIP4	4B5> 10C4<
TTIP5	5B8> 11C8<
TTIP6	5B4> 11C4<
TTIP7	6B8> 12C8<
TTIP8	6B4> 12C4<
WE_T	14C2< > 16C6< >
WR_RW	14C2< > 2B7< 7C7< 8C6<
XRST	13A6> 13C2<
X_INIT	13A6< > 14A5< > 14D8< >

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*** Part Cross-Reference for the entire design ***

C1	CAP1	9B7
C2	CAP1	9C7
C3	CAP1	9B3
C4	CAP1	9C3
C5	CAP1	10B7
C6	CAP1	10C7
C7	CAP1	10B3
C8	CAP1	10C3
C9	CAP1	11B7
C10	CAP1	11C7
C11	CAP1	11B3
C12	CAP1	11C3
C13	CAP1	12B7
C14	CAP1	12C7
C15	CAP1	12B3
C16	CAP1	12C3
C17	CAP1	14C8
C18	CAP1	14D6
C19	CAP1	14D6
C20	CAP1	14D6
C21	CAP1	14D6
C22	CAP1	14D6
C23	CAP1	16A7
C24	CAP1	16A7
C26	CAP1	16A6
C28	CAP1	16A6
C29	CAP1	16A6
C30	CAP1	16A5
C31	CAP1	16A5
C35	CAP1	16A5
C36	CAP1	16A4
C37	CAP1	16A4
C38	CAP1	16A4
C39	CAP1	16A4
C40	CAP1	16A4
C41	CAP1	16A4
C42	CAP1	16A3
DS1	LED	14B1
DS2	LED	3C7
DS3	LED	3C6
DS4	LED	3C3
DS5	LED	3C2
DS6	LED	4C7
DS7	LED	4C6
DS8	LED	4C3
DS9	LED	4C3
DS10	LED	5C7
DS11	LED	5C6
DS12	LED	5C3
DS13	LED	5C2
DS14	LED	6C7
DS15	LED	6C6
DS16	LED	6C3
DS17	LED	6C2
DS18	LED	14B6
J1	CONN_BNC_5P	9D5
J2	RJ45_8	9C1 9C5 10C1 10C5
J3	CONN_BNC_5P	9B5
J4	CONN_BNC_5P	9D1
J5	CONN_BNC_5P	9B1
J6	CONN_BNC_5P	10D5
J7	CONN_BNC_5P	10B5
J8	CONN_BNC_5P	10D1
J9	CONN_BNC_5P	10B1
J10	CONN_BNC_5P	11D5
J11	RJ45_8	11C1 11C5 12C1 12C5
J12	CONN_BNC_5P	11B5
J13	CONN_BNC_5P	11D1
J14	CONN_BNC_5P	11B1
J15	CONN_BNC_5P	12D5
J16	CONN_BNC_5P	12B5
J17	CONN_BNC_5P	12D1
J18	CONN_BNC_5P	12B1
J19	CONN_50P2	16D7
J20	CONN_50P2	16D3
J21	CONN_20P	3D5
J22	CONN_10P	3C5
J23	CONN_20P	3D1
J24	CONN_10P	3B1
J25	CONN_20P	4D5
J26	CONN_10P	4C5
J27	CONN_20P	4D1
J28	CONN_10P	4B1
J29	CONN_20P	5D5
J30	CONN_10P	5C5
J31	CONN_20P	5D1
J32	CONN_10P	5B1
J33	CONN_20P	6D5
J34	CONN_10P	6B5
J35	CONN_20P	6D1
J36	CONN_10P	6B1
JP1	CON12P	13B7
R1	RES1	9C8
R2	RES1	9C8
R3	RES1	9B8
R4	RES1	9B7
R5	RES1	9D4
R6	RES1	9C4
R7	RES1	9B4
R8	RES1	9B3
R9	RES1	10C8
R10	RES1	10C8
R11	RES1	10B8
R12	RES1	10B7
R13	RES1	10D4
R14	RES1	10C4
R15	RES1	10B4
R16	RES1	10B3
R17	RES1	11C8
R18	RES1	11C8
R19	RES1	11B8
R20	RES1	11B7
R21	RES1	11D4
R22	RES1	11C4
R23	RES1	11B4
R24	RES1	11B3
R25	RES1	12C8
R26	RES1	12C8
R27	RES1	12B8
R28	RES1	12B7
R29	RES1	12D4
R30	RES1	12C4
R31	RES1	12B4
R32	RES1	12B3
R33	RES1	13A8
R34	RES1	14D8
R35	RES1	13A6
R36	RES1	13C1
R37	RES1	14B2
R38	RES1	2C2
R39	RES1	3B7
R40	RES1	3B6
R41	RES1	3B3
R42	RES1	3B2
R43	RES1	4B7
R44	RES1	4C6
R45	RES1	4B3
R46	RES1	4B3
R47	RES1	5C7
R48	RES1	5C6
R49	RES1	5B3
R50	RES1	5B2
R51	RES1	6C7
R52	RES1	6C6
R53	RES1	6C3
R54	RES1	6C3
R55	RES1	14C2
R56	RES1	14C2
R57	RES1	14C1
R58	RES1	14C1
R59	RES1	3A6
R60	RES1	3A3
R61	RES1	4A7
R62	RES1	4A3
R63	RES1	5A7
R64	RES1	5A2
R65	RES1	6A7
R66	RES1	6A2
R67	RES1	14B1
R68	RES1	14A7
T1	XFMR_2IN_4OUT	9B6 9C6
T2	XFMR_2IN_4OUT	9B2 9D2
T3	XFMR_2IN_4OUT	10B6 10C6
T4	XFMR_2IN_4OUT	10B2 10D2
T5	XFMR_2IN_4OUT	11B6 11C6
T6	XFMR_2IN_4OUT	11B2 11D2
T7	XFMR_2IN_4OUT	12B6 12C6
T8	XFMR_2IN_4OUT	12B2 12D2
U1	DS26401_U2	2B5 3D3 3D7 4D4 4D8 5D3 5D8 6D4 6D8
U2	DS2144B_QFP	3B4 3B8 4B4 4B8 7C5
U3	DS2144B_QFP	5B4 5B8 6B4 6B8 8C5
U4	XC18V02VQ44C_U	13A5
U6	MAX1792	14D7
U7	XC2S50BGA_U	13C4 14B4 15C5

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